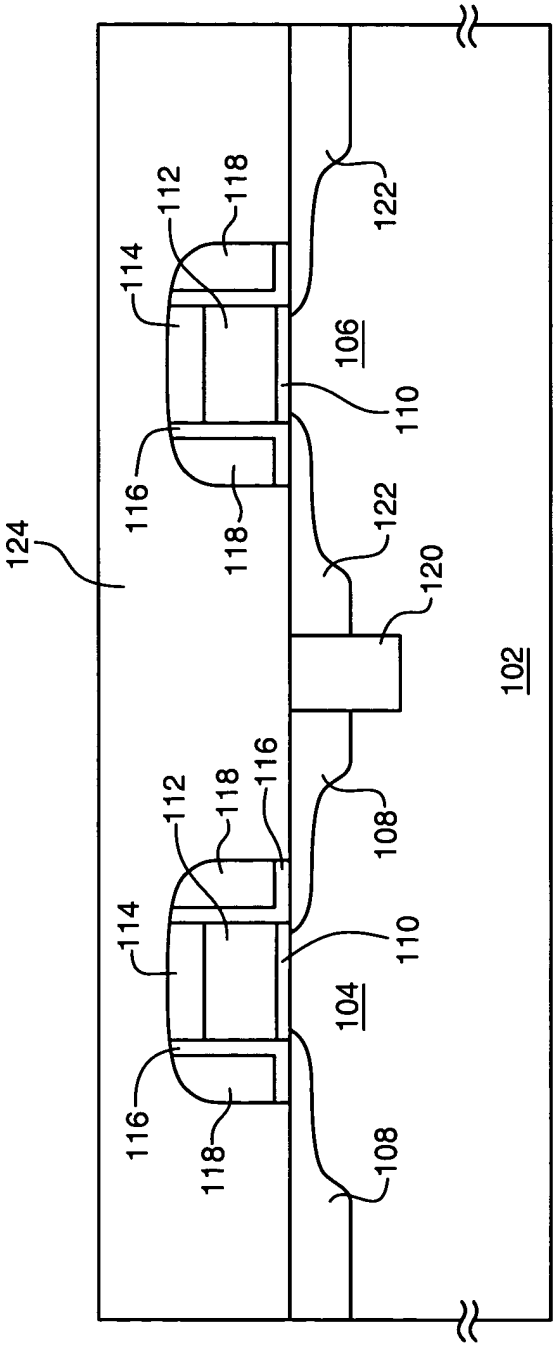


FIG. 1
PRIOR ART

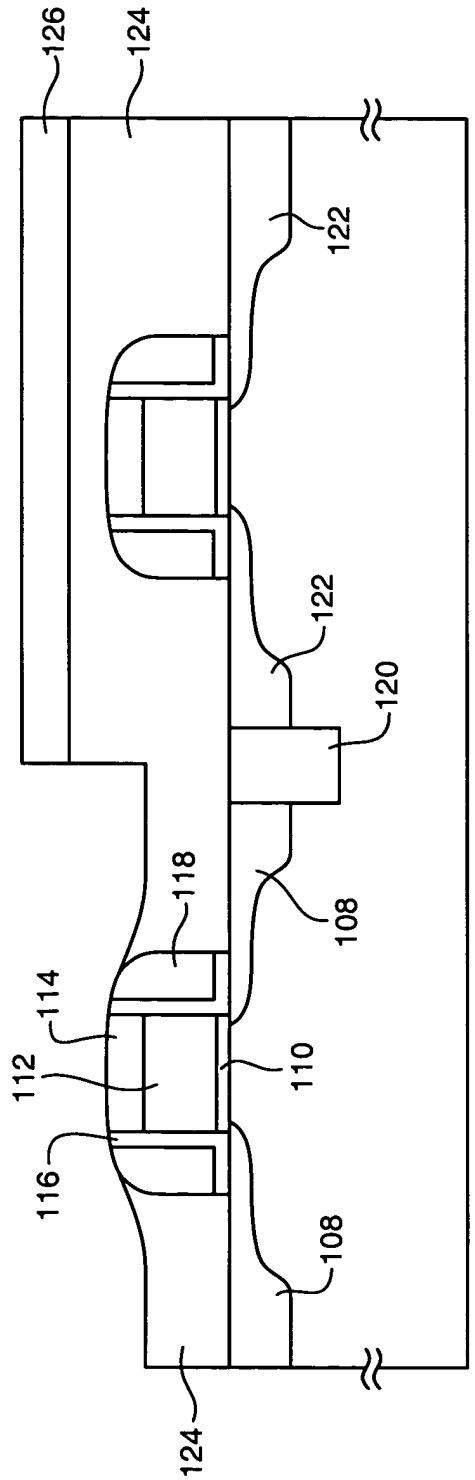


FIG. 2

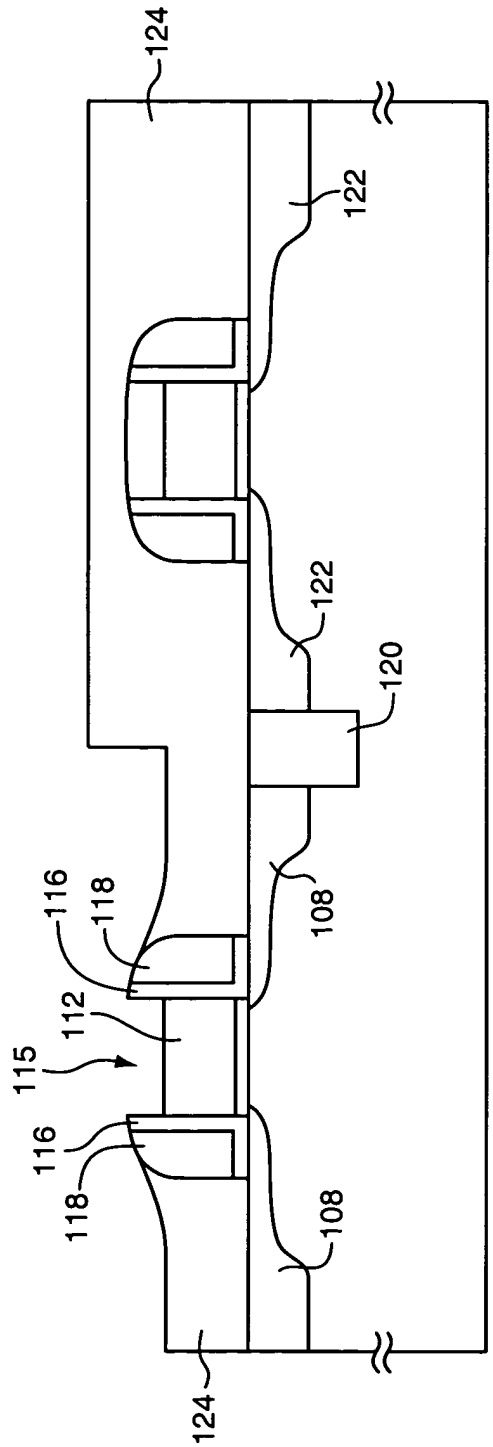


FIG. 3

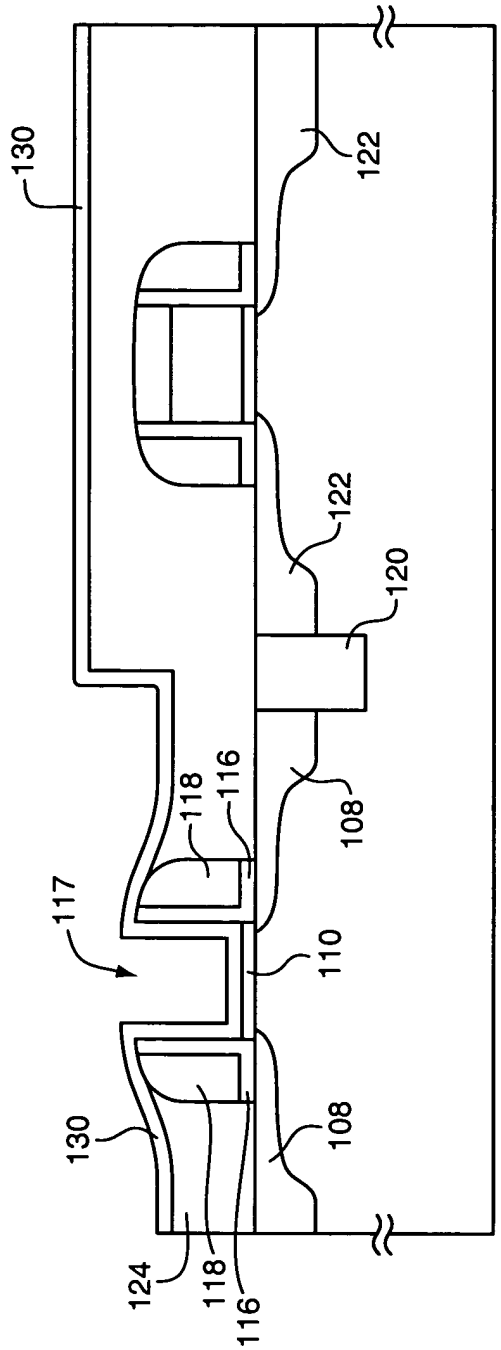


FIG. 4

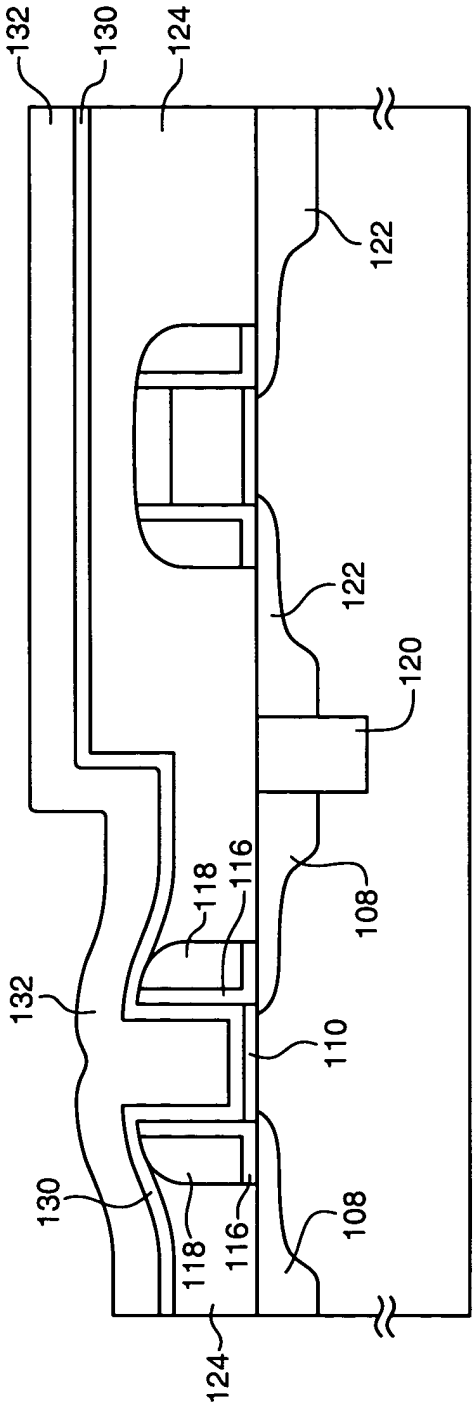


FIG. 5

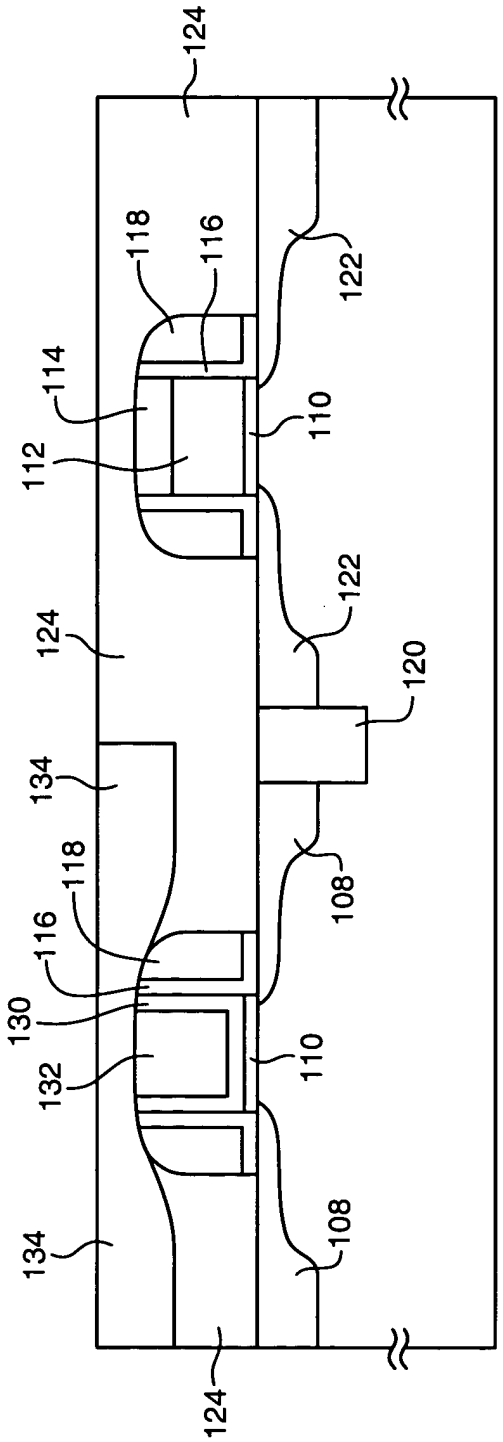

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FIG. 6

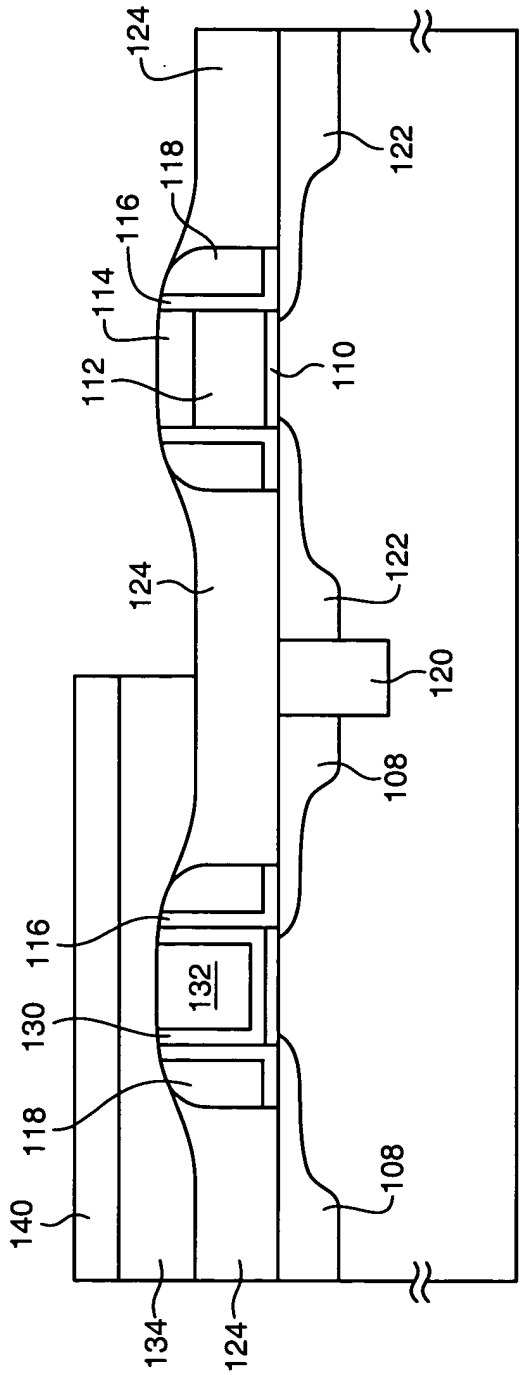

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FIG. 7

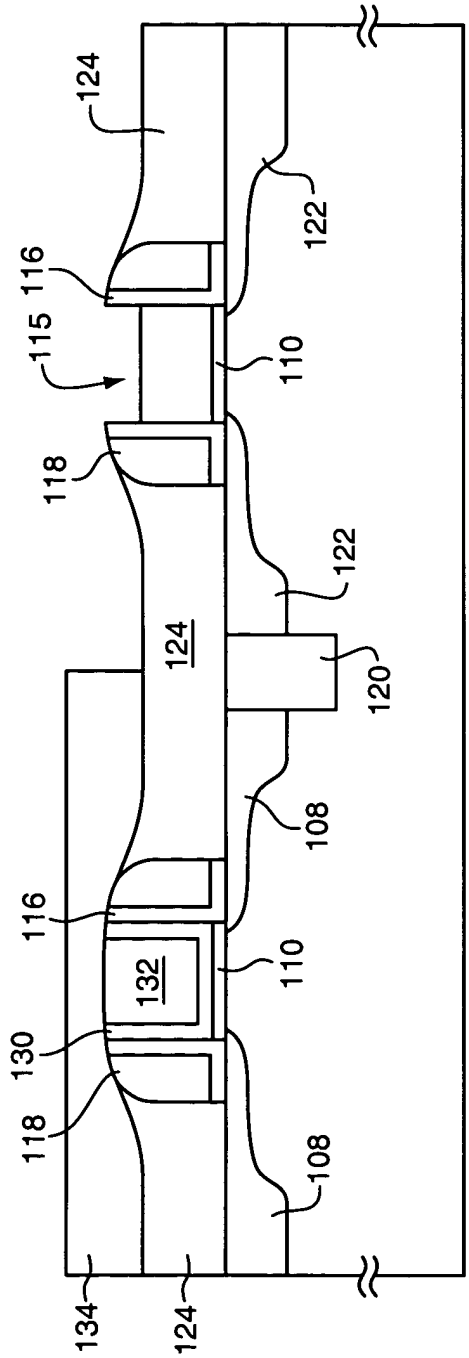

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FIG. 8

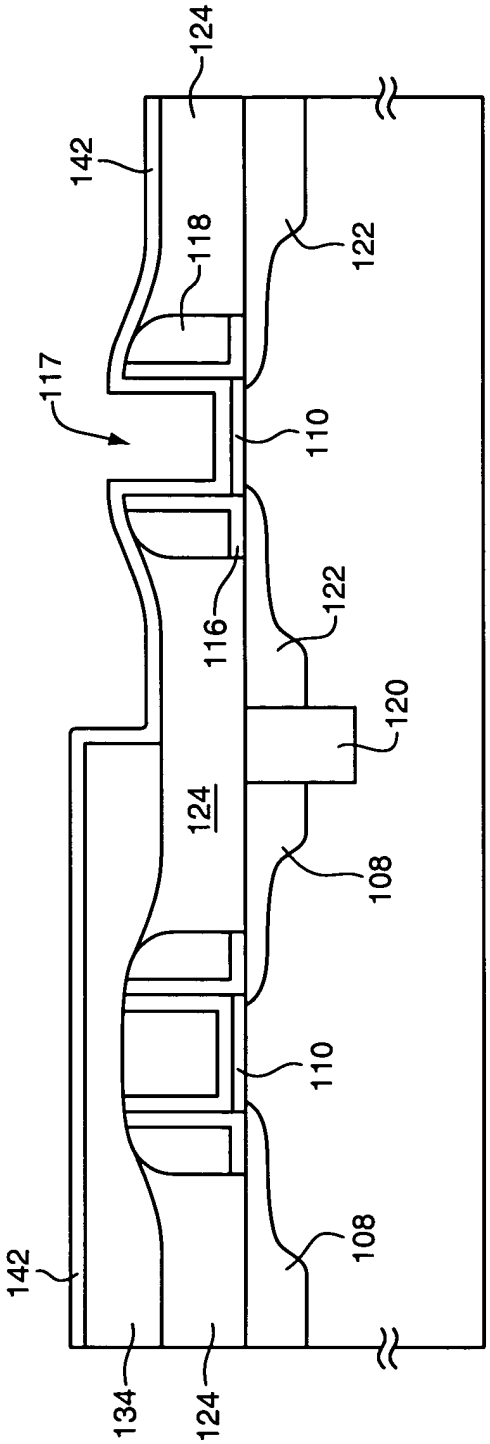


FIG. 9

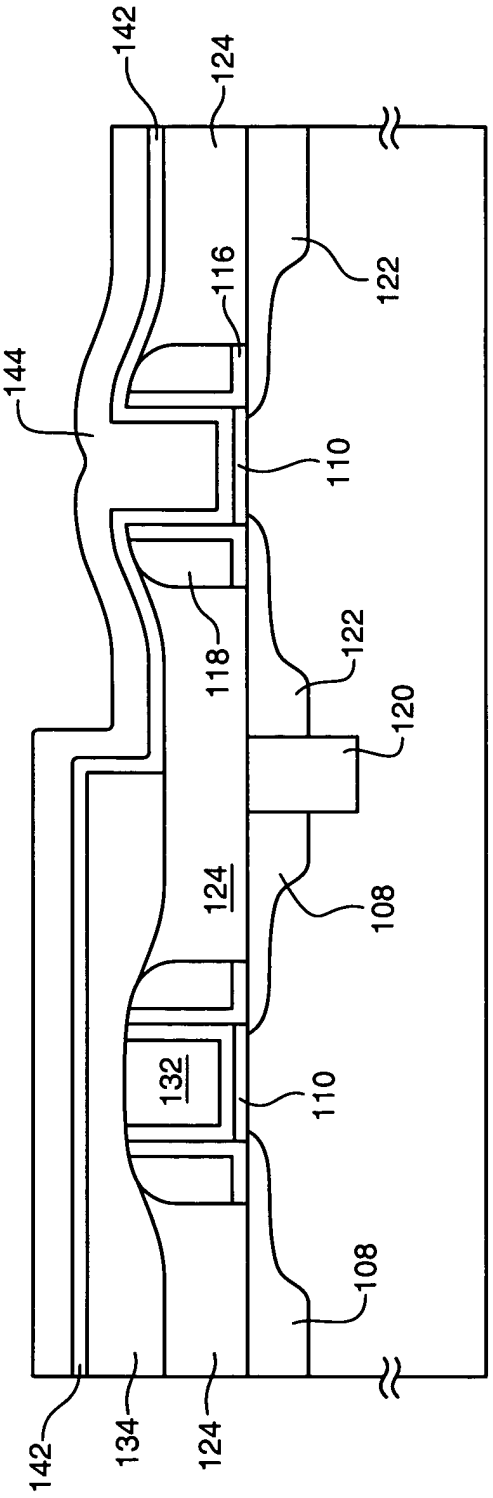

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FIG. 10

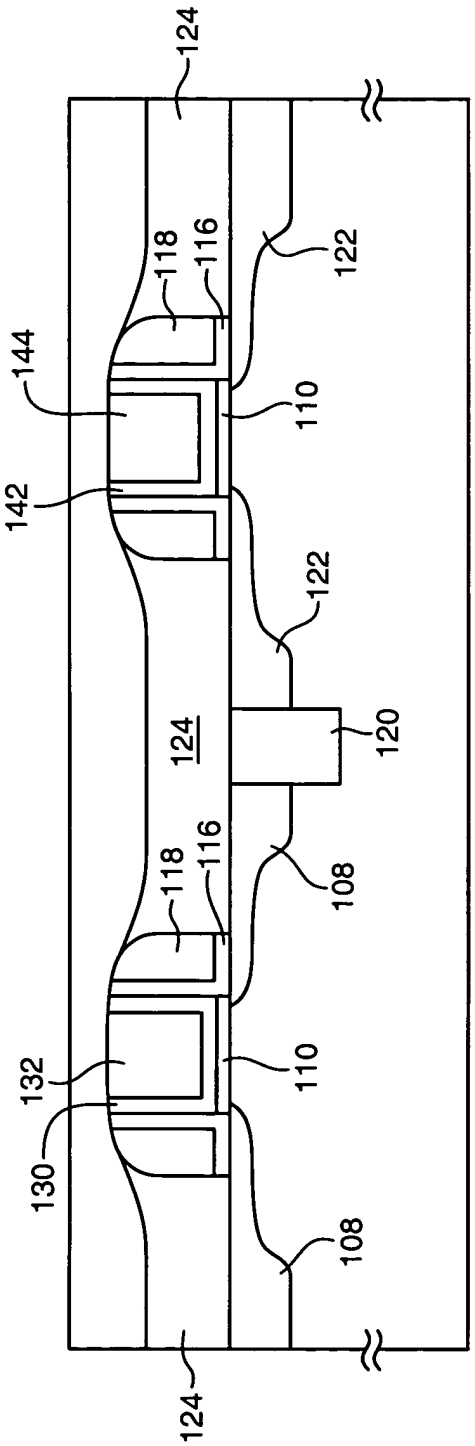

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FIG. 11

FIG. 12

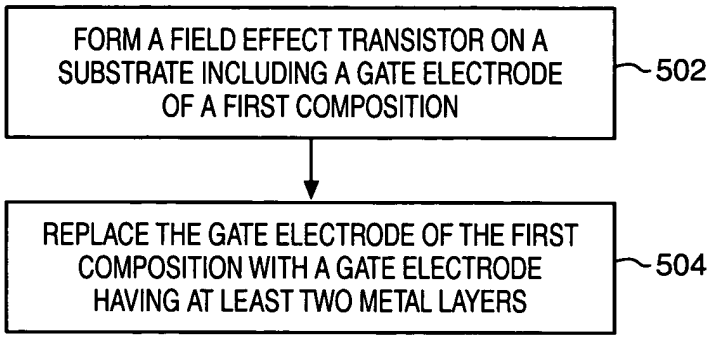
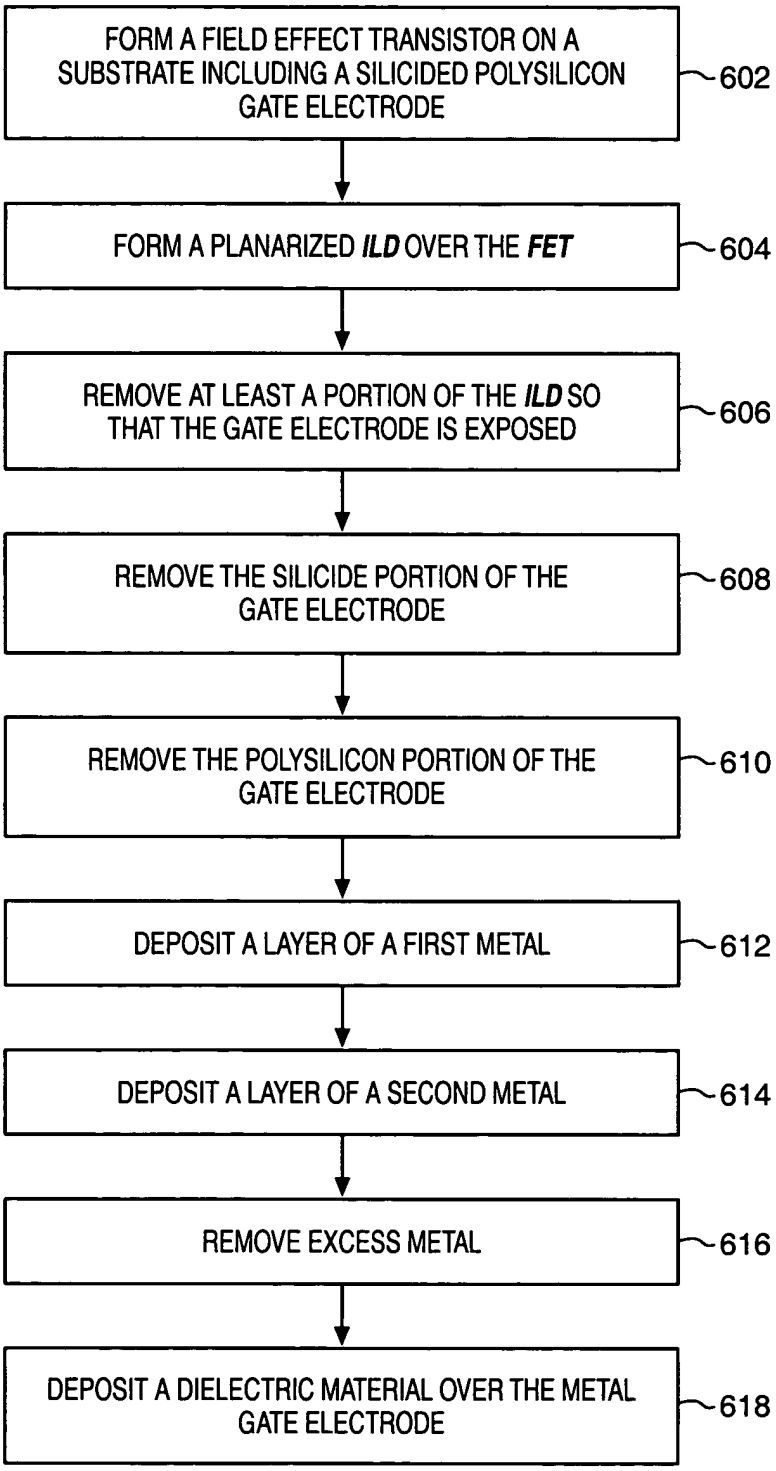

FORM A FIELD EFFECT TRANSISTOR ON A SUBSTRATE INCLUDING A GATE ELECTRODE OF A FIRST COMPOSITION
502
REPLACE THE GATE ELECTRODE OF THE FIRST COMPOSITION WITH A GATE ELECTRODE HAVING AT LEAST TWO METAL LAYERS
504

FIG. 13


FORM A FIELD EFFECT TRANSISTOR ON A SUBSTRATE INCLUDING A SILICIDED POLYSILICON GATE ELECTRODE
602
FORM A PLANARIZED *ILD* OVER THE *FET*
604
REMOVE AT LEAST A PORTION OF THE *ILD* SO THAT THE GATE ELECTRODE IS EXPOSED
606
REMOVE THE SILICIDE PORTION OF THE GATE ELECTRODE
608
REMOVE THE POLYSILICON PORTION OF THE GATE ELECTRODE
610
DEPOSIT A LAYER OF A FIRST METAL
612
DEPOSIT A LAYER OF A SECOND METAL
614
REMOVE EXCESS METAL
616
DEPOSIT A DIELECTRIC MATERIAL OVER THE METAL GATE ELECTRODE
618